

In the Claims

1 1.-20. (Canceled)

2 21. (Original) An isolation structure in a semiconductor substrate comprising:
3 a semiconductor substrate;
4 a plurality of adjacent trenches in said semiconductor substrate; and
5 a self-aligned isolation structure in upper portions of selected ones of said
6 plurality of trenches, said isolation structure being merged portions of
7 said semiconductor substrate along at least a first row of said selected
8 ones of said plurality of adjacent trenches, said merged portions of said
9 semiconductor substrate being aligned as-formed to edges of said
10 plurality of adjacent trenches,
11 wherein said self-aligned isolation structure isolates a first region of said
12 semiconductor substrate from a second region of said semiconductor substrate.

1 22. (Previously presented) The structure of claim 21 wherein said
2 semiconductor substrate comprises a silicon substrate.

1 23. (Previously presented) The structure of claim 21 further including a pad
2 dielectric layer thereover a surface of said semiconductor substrate.

1 24. (Previously presented) The structure of claim 23 wherein said pad
2 dielectric layer comprises a pad oxide layer followed by a pad nitride layer.

1 25. (Previously presented) The structure of claim 24 wherein said pad oxide
2 layer has a thickness ranging from about 1 nm to about 10 nm.

1 26. (Previously presented) The structure of claim 24 wherein said pad nitride
2 layer has a thickness ranging from about 50 nm to about 500 nm.

1 27. (Previously presented) The structure of claim 21 wherein said plurality of
2 adjacent trenches have depths ranging from about 250 nm to about 10 μ m.

1 28. (Previously presented) The structure of claim 21 wherein said self-aligned
2 isolation structure comprises a thermal oxide region existing along said at least first
3 row of selected ones of said plurality of adjacent trenches.

1 29. (Previously presented) The structure of claim 28 wherein said
2 semiconductor substrate comprises a silicon substrate and said thermal oxide
3 region comprises a thermal silicon dioxide region existing along said at least first
4 row of selected ones of said plurality of adjacent trenches.

1 30. (Original) An isolation structure in a semiconductor substrate comprising:

2 a silicon substrate having a layer of pad oxide disposed thereover said silicon
3 substrate and a layer of pad nitride disposed thereover said pad oxide;
4 a plurality of adjacent trenches traversing through said pad oxide, said pad
5 nitride, and stopping in said silicon substrate; and
6 a self-aligned, thermal oxide isolation structure in upper portions of said
7 plurality of adjacent trenches, said thermal oxide isolation structure being
8 oxidized portions of said semiconductor substrate merged along at least a
9 first row of selected ones of said plurality of adjacent trenches in said
10 upper portions of said trenches, said oxidized portions of said
11 semiconductor substrate being aligned as-formed to edges of said
12 plurality of adjacent trenches,
13 wherein said thermal oxide isolation structure isolates a first region of said
14 semiconductor substrate from a second region of said semiconductor substrate.

15 31. (Currently Amended) An isolation structure in a semiconductor substrate
16 comprising:
17 a semiconductor substrate;
18 a plurality of adjacent trenches in said semiconductor substrate having depths
19 ranging from about 250 nm to about 10 μ m;
20 a plurality of adjacent segments of said semiconductor substrate between each
21 of said plurality of adjacent trenches;

22 an oxidation barrier layer residing in lower portions of said plurality of adjacent
23 trenches;
24 a self-aligned shallow trench isolation comprising merged sections of selected
25 ones of said plurality of adjacent segments of said semiconductor substrate
26 along a first row above said oxidation barrier layer.

1 32. (Previously presented) The structure of claim 31 wherein said
2 semiconductor substrate comprises a silicon substrate.

1 33. (Previously presented) The structure of claim 31 further including a pad
2 dielectric layer thereover a surface of said semiconductor substrate.

1 34. (Previously presented) The structure of claim 33 wherein said pad
2 dielectric layer comprises a pad oxide layer followed by a pad nitride layer.

1 35. (Previously presented) The structure of claim 31 wherein said oxidation
2 barrier layer is a material selected from the group consisting of local oxidation of
3 silicon, silicon nitride and silicon oxynitride.

1 36. (Currently Amended) The structure of claim ~~33~~31 wherein said oxidation
2 barrier layer has a thickness ranging from about 2nm to about 50nm.

1 37. (Canceled)

1 38. (Previously presented) The structure of claim 31 wherein said self-aligned
2 isolation structure comprises a thermal oxide region existing along said at least first
3 row of selected ones of said plurality of adjacent trenches.

1 39. (Previously presented) The structure of claim 38 wherein said
2 semiconductor substrate comprises a silicon substrate and said thermal oxide
3 region comprises a thermal silicon dioxide region existing along said at least first
4 row of selected ones of said plurality of adjacent trenches.

1 40. (Previously presented) The structure of claim 31 wherein said selected ones
2 of said plurality of adjacent segments of said semiconductor substrate comprise
3 those adjacent segments of said semiconductor substrate along said at least first
4 row having a thinned diameter ranging from about $1/5$ to about $1/2$ that of a non-
5 thinned, original diameter of said plurality of adjacent segments of said
6 semiconductor substrate.